CLAIMS

1. A self testing imager including:

a controller outputting a sewer signal and a read signal; and

a pixel array connected to the controller including a plurality of pixels, each pixel including a sewer for injecting a charge into the pixel in response to the sewer signal, and an output node;

wherein the pixel outputs an injected output signal representing the injected charge in response to the read signal, the controller comparing the injected output signal to an expected output signal to test the operation of the pixel.

2. The imager of claim 1, each pixel further including a collect gate for receiving a collect signal from the controller, and a collect well associated with the collect gate for receiving the injected charge from the sewer in response to the collect signal.

3. The imager of claim 1, each pixel further including a read gate for receiving the read signal, and a read well associated with the read gate for receiving the injected charge from the sewer in response to the read signal.

4. The imager of claim 3, each pixel further including a transistor having a gate coupled to the read well, a drain connected to the controller to receive the read signal, and a source coupled to the output node, the read signal being modulated by the injected charge at the gate of the transistor to produce the injected output signal.

5. The imager of claim 1, each pixel further including a dump gate for receiving a dump signal from the controller, the injected charge being dumped to the sewer in response to the dump signal and removal of the read signal and the sewer signal, thereby leaving a background charge.

6. The imager of claim 5 wherein the pixel outputs the background signal representing the background charge in response to the read signal, the controller comparing the injected output signal to the background output signal as part of a correlated double sampling procedure.

7. The imager of claim 1 further including a read-out circuit having a plurality of flip-flops and a plurality of buffers enabled by the flip-flops to transfer the injected output signal from the pixels to the controller.

8. The imager of claim 7 wherein the pixels are arranged in rows and columns in the pixel array, each buffer having an input connected to all of the pixels in a column of pixels associated with the buffer and an output connected to the controller, a first quantity of the plurality of buffers being connected to odd numbered columns and a second quantity of the plurality of buffers being connected to even numbered columns.

9. The imager of claim 8 wherein the plurality of flip-flops are sequentially enabled by a plurality of clock pulses from the controller, a first quantity of the plurality of flip-flops being connected to the first quantity of buffers, a second quantity of the plurality of flip-flops being connected to the second quantity of buffers.

10. The imager of claim 9 wherein each flip-flip enables a pair of buffers in response to a clock pulse, each clock pulse resulting in a transfer of the injected output signal from four adjacent columns of pixels to the controller.

11. A self testing imager including:

a controller; and

a plurality of pixels, each pixel including a collect well, a dump gate connected to the controller for receiving a dump signal, a sewer connected to the controller for receiving a sewer signal, the sewer injecting a predetermined charge into the collect well when the sewer signal and the dump signals are in a first state, and a read well coupled to the controller for receiving the injected charge from the collect well and providing the injected charge as an output signal through an output node to the controller,

wherein the controller compares the output signal to an expected signal related to the injected charge to test the operation of the pixel.

12. The imager of claim 11, each pixel further including a collect gate disposed adjacent the collect well and connected to the controller for receiving a collect signal, and a floating gate disposed adjacent the read well.

13. The imager of claim 12, each pixel further including a transistor having a gate connected to the floating gate, a drain connected to the controller for receiving the read signal, and a source coupled to the output node, the injected charge being transferred from the collect well to the read well to the floating gate when the collect signal is in a second state and the read signal is in a first state, the injected charge at the floating gate modulating the read signal conducted through the transistor, the output signal being equal to the modulated read signal.

14. The imager of claim 12 wherein the sewer, the collect well, and the read well are disposed in a silicon substrate, the collect gate and the floating gate being first layer polysilicon gates.

15. The imager of claim 12, each pixel further including a read gate connected to the controller for receiving a read signal, the floating gate being disposed between the read gate and the read well.

16. The imager of claim 15 wherein the dump gate and the read gate are second layer polysilicon gates.

17. The imager of claim 15 wherein the collect gate is disposed between the dump gate, the read gate, and the collect well, the dump gate and the read gate defining an opening adjacent the collect gate, the pixel receiving incident light through the opening, the light having photons which pass through the collect gate and deposit electrons in the collect well when the collect and dump signals are in a first state and the sewer signal is in a second state, thereby creating an image charge.

18. The imager of claim 17 wherein the image charge is transferred from the collect well to the read well when the collect signal is in a second state and the read signal is in a first state.

19. The imager of claim 17 wherein the collect well dumps the image signal to the sewer when the read and sewer signals are in the second state and the collect and dump signals are in the first state.

20. A self testing imager including:

a controller outputting a sewer signal, a collect signal, and a read signal; and

a pixel array connected to the controller including a plurality of pixels, each pixel including

a collect well for receiving a charge in response to application of the collect signal to the pixel,

a sewer for receiving the sewer signal, the sewer injecting a charge into the collect well in response to the concurrent application of the sewer signal and the collect signal to the pixel,

a read well for receiving the injected charge from the collect well in response to application of the read signal to the pixel and the absence of the collect signal, and

a transistor having a gate coupled to the read well, a drain for receiving the read signal, and a source coupled to an output node connected to the controller;

wherein the read signal is modulated by the injected charge at the transistor gate, thereby generating an injected output signal at the output node representing the injected charge, the controller comparing the injected output signal to an expected output signal to test the operation of the pixel.

21. The imager of claim 20, each pixel further including a substrate, the collect well, the sewer, and the read well being disposed in the substrate.

22. The imager of claim 20, each pixel further including a collect gate adjacent the collect well connected to the controller, the collect gate creating the collect well in response to application of the collect signal to the collect gate.

23. The imager of claim 22, each pixel further including a read gate adjacent the read well connected to the controller, the read gate creating the read well in response to application of the read signal to the read gate.

24. The imager of claim 23, each pixel further including a floating gate disposed between the read gate and the read well, the floating gate transferring the injected charge from the read well to the transistor gate in response to the read signal.

25. A self testing imager including:

a controller; and

a plurality of pixels connected to the controller, each pixel including

a collect well, a sewer, a dump gate, and a read well, each having a first and a second state,

the collect well collecting an image charge when in the first state,

the read well receiving the image charge when the collect well is in the second state and the read well is in the first state,

the collect well dumping the image charge to the sewer when the collect well is in the second state, and the dump gate and the sewer are each in the first state,

the sewer providing an injected charge to the collect well when the sewer is in the second state and the dump gate and the collect well are each in the first state,

the read well receiving the injected charge when in the collect well is in the second state and the read well is in the first state;

wherein the controller reads the image charge and the injected charge by applying a read signal to the pixel, and compares the injected charge to an expected charge to test the operation of the pixel.

26. A method of testing the operation of an imager having a plurality of pixels, the method including the steps of:

outputting a first electrical signal to each pixel to inject a known charge into the pixel;

outputting a second electrical signal to each pixel to read an output signal representing the injected charge; and

comparing the output signal to an expected output signal to test the operation of each pixel.

27 The method of claim 26 further including the step outputting a third electrical signal to each pixel while outputting the first signal to inject the known charge.

28. The method of claim 27 further including the step of outputting a fourth electrical signal to each pixel while outputting the first and third signals to inject the known charge.

29. The method of claim 28 further including the step of removing the third signal while outputting the first and fourth signals to inject the known charge.

30. The method of claim 29 further including the step of removing the first and fourth signals while outputting the second signal to read the output signal.

31. The method of claim 26 further including the steps of outputting a third electrical signal and a fourth electrical signal to each pixel to inject the known charge, and removing the second signal, then the fourth signal, and then the third signal to erase the injected charge.32.

The method of claim 31 further including the step of outputting another second signal to read a second output signal representing the erased injected charge.

33. The method of claim 26 wherein the plurality of pixels is arranged in an array having a plurality of rows of pixels and a plurality of columns of pixels, the read signal being concurrently provided to a row of pixels at a time, each row of the array sequentially receiving the read signal.